REMARKS

The Office Action mailed October 24, 2002, has been received and reviewed. Claims 23 through 33 are currently pending in the application. All claims stand rejected. Claim 30 has been objected to based upon an informality. Applicants have amended each of claims 23 through 33 and respectfully request reconsideration of the application as amended herein.

Drawings

Applicants submit herewith a Transmittal of Formal Drawings, under separate cover, and formal drawings. Applicants respectfully request approval of the formal drawings.

Claim Objection

Claim 30 has been objected to based upon an inadvertent informality. Specifically, claim 30 has been objected to based upon the phrase "a non-crystalline" at line 5 thereof. The objected to phrase has been amended herein to recite "said non-crystalline" for clarity as suggested by the Examiner. Accordingly, it is respectfully submitted that the objection has been overcome.

35 U.S.C. § 102(e) Anticipation Rejection

A) Applicable Authority

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

B) Anticipation Rejection Based on U.S. Patent 5,472,896 to Chen et al.

Claims 23 through 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 5,472,896 to Chen et al. (hereinafter the "Chen reference"). As the Chen reference fails to disclose, either expressly or inherently, each and every element as set forth in the claims, as amended herein, Applicants respectfully traverse this rejection.

The Chen reference discloses, in a first embodiment, a MOSFET device, and method for fabricating the same, having a gate oxide layer 12 formed over a semiconductor substrate 10, a polysilicon layer 14 formed over the gate oxide layer 12 and a refractory metal silicide layer 16 formed over the polysilicon layer 14. *See, Chen reference*, col. 1, line 57–col. 2, line 5; col. 4, lines 29-36; FIG. 3b. In fabricating the device of the first embodiment, subsequent to formation of the metal silicide layer 16, the structure is etched down to the gate oxide layer 12 as shown in FIG. 3b. Subsequently, a first thin oxide layer 18 is formed over the exposed surfaces of the gate oxide layer 12, the polysilicon layer 14, the metal silicide layer 16 and the semiconductor substrate 10 by thermal oxidation. This thermal treatment transforms the metal silicide layer 16 from its amorphous form into a crystalline form. *See id.*, col. 2, lines 14–20; FIGs. 3c and 4c. Next, a second oxide layer 20 is formed over the first thin oxide layer 18 and the two oxide layers 18, 20 are etched back to form sidewall spacers 20 on the side walls of the gate electrode structure. *See id.*, col. 2, lines 26-34. After formation of the sidewall spacers 20, an ion implantation step is performed to transform the metal silicide layer 16 from its crystalline form back into the amorphous form. *See id.*, col. 4, lines 36-42.

In a second embodiment, the MOSFET device of the Chen reference further includes a barrier cap layer 30 formed over the refractory metal silicide layer 16, preferably by chemical vapor deposition (CVD). *See id.*, col. 4, line 65–col. 5, line 8; FIG. 4b. Due to the thermal treatment of the CVD process, the metal silicide layer 16 is transformed from the amorphous form into a crystalline form upon deposition of the barrier cap layer 30. *See id.* In fabricating the device of this second embodiment, subsequent to deposition of the barrier cap layer 30 (and thus transformation from the amorphous form into a crystalline form), the barrier cap layer 30, the metal silicide layer 16 and the polysilicon layer 14 are etched down to the gate oxide layer 12

as shown in FIG. 4b. After formation of the gate electrode structure, ion implantation is performed to transform the metal silicide layer 16 back into the amorphous form. *See id.*, col. 5, lines 9-25. The MOSFET device is then completed as described above with regard to the first embodiment.

As recognized by both the Specification of the present application and the Chen reference, high temperature steps during fabrication of gate stack structures (*e.g.*, thermal oxidation, CVD and the like) cause the formation of silicon clusters within the metallic silicide film. *See, Specification*, page 5, lines 19-21; *Chen reference*, col. 2, lines 49-53 and col. 5, lines 5-8. The Specification of the present application indicates pitting is caused on the dielectric layer during gate stack etching by the presence of such silicon clusters inside the metallic silicide film. *See, Specification*, page 5, lines 24–26. Specifically, the etch rate of silicon clusters has been found to be approximately 1.2 times that of the metallic silicide film (in the case of tungsten silicide film) during gate stack etch. Accordingly, the silicon clusters etch tunnels into the metallic silicide film at each silicon cluster. This tunneling is, in turn, translated into the surface of the gate dielectric layer and, thereby, pits are formed. *See id.*, page 5, line 24–page 6, line 2. If the pits are deep enough to extend through the gate dielectric layer and into the silicon substrate, junction leakage, refresh problems and potential destruction of the component may occur. *See id.*, page 3, line 27–page 4, line 2.

It is respectfully submitted that the Chen reference fails to disclose, either expressly or inherently, a gate stack or semiconductor device comprising a gate stack, on a silicon substrate, having a dielectric layer thereover, wherein the dielectric layer is substantially devoid of pitting and wherein the gate stack includes a dielectric cap on a metallic silicide film, as claimed in the present application.

Independent claim 23, as amended herein, recites an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. The operable gate stack includes a non-crystalline metallic silicide film and a dielectric cap on the non-crystalline metallic silicide film. As previously stated, the first embodiment disclosed in the Chen reference does not include a dielectric cap on the non-crystalline metallic

silicide film. Accordingly, it is respectfully submitted that such embodiment does not anticipate amended independent claim 23. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

With regard to the second embodiment of the Chen reference, it is respectfully submitted that the dielectric layer of the MOSFET device so described is not "substantially devoid of pitting" as recited in independent claim 23. As previously described, during formation of the device of the second embodiment described in the Chen reference, the gate electrode structure is etched *subsequent to* deposition of the barrier cap layer 30 and *prior to* ion implantation being performed on the metal silicide layer 16. *See, Chen reference*, col. 4, line 65–col. 5, line 8; FIG. 4b. Upon deposition of the barrier cap layer 30, silicon crystals are formed in the metal silicide layer 16. *See id.* Accordingly, when the gate electrode structure is subsequently etched, silicon crystals are present in the metal silicide layer 16. Only after etching of the gate electrode structure is the metal silicide layer 16 implanted with ions to transform the metal silicide layer back into the amorphous state. *See id.*, col. 5, lines 9-25. Thus, since the gate electrode structure is etched *while the silicon crystals are present in the metal silicide layer 16*, it is respectfully submitted that the dielectric layer contains pits caused by the difference in the etch rate of the silicon crystals relative to the metallic silicide film. *See, Specification*, page 5, line 24 – page 6, line 2.

It is stated in the outstanding Office Action "that because a metallic silicide film (16) is in [an] amorphous state, it is inherent that the dielectric layer is substantially devoid of pitting." Office Action, page 3, ¶4. Applicants respectfully disagree. Ion implantation subsequent to etching the gate electrode structure to amorphize the metal silicide layer 16 substantially eliminates the silicon crystals from the metal silicide layer 16 but does ***not*** eliminate the pitting already caused by the gate etch. Accordingly, it is respectfully submitted that the MOSFET structure of the second embodiment of the Chen reference contains pitting in the dielectric layer and thus does not anticipate amended independent claim 23 of the present application.

Independent claim 24, as amended herein, recites an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of

pitting. The operable gate stack includes an amorphous metallic silicide film which is substantially devoid of silicon clusters and a dielectric cap on the amorphous metallic silicide film. As discussed with regard to claim 23 above, it is respectfully submitted that the first embodiment disclosed by the Chen reference fails to describe, either expressly or inherently, an operable gate stack having a dielectric cap on a non-crystalline silicide film.

Further, it is respectfully submitted that the second embodiment disclosed by the Chen reference fails to describe, either expressly or inherently, an operable gate stack on a silicon substrate having a dielectric layer thereover, *the dielectric layer being substantially devoid of pitting*. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched prior to implanting the metal silicide layer and transforming it back to the amorphous state. Thus, amended independent claim 24 is not anticipated by the Chen reference.

Independent claim 25, as amended herein, recites an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. The operable gate stack comprises a polysilicon layer disposed over the dielectric layer, a non-crystalline metallic silicide film disposed over the polysilicon layer and a dielectic cap on the non-crystalline metallic silicide film. It is respectfully submitted that the first embodiment of the Chen reference fails to disclose, either expressly or inherently, an operable gate stack comprising, in part, a dielectric cap on a non-crystalline metallic silicide film as recited in amended independent claim 25. Accordingly, it is respectfully submitted that amended independent claim 25 is not anticipated by the first embodiment disclosed by the Chen reference.

Further, the Chen reference fails to disclose, either expressly or inherently, in the second embodiment thereof, an operable gate stack on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched prior to implanting the metal silicide layer and transforming it back to the amorphous state. As such, it is respectfully submitted that amended independent claim 25 is not anticipated by the second embodiment disclosed by the Chen reference.

Independent claim 26, as amended herein, recites a gate stack structure comprising an operable gate stack on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially devoid of pitting. The operable gate stack of claim 26 comprises a metallic silicide film and a dielectric cap on the metallic silicide film. It is respectfully submitted that the Chen reference, in the first embodiment disclosed therein, fails to describe, either expressly or inherently, a gate stack structure comprising an operable gate stack, the gate stack comprising a dielectric cap on a metallic silicide film. As such, amended independent claim 26 is not anticipated by the first embodiment of the Chen reference.

Regarding the second embodiment disclosed by the Chen reference, it is respectfully submitted that a gate stack structure comprising an operable gate stack on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially devoid of pitting is not described, either expressly or inherently. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched prior to implanting the metal silicide layer and transforming it back to the amorphous state. Accordingly, it is respectfully submitted that amended independent claim 26 is not anticipated by the second embodiment of the Chen reference.

Independent claim 29, as amended herein, recites a semiconductor device comprising at least one gate stack which comprises a non-crystalline metallic silicide film and a dielectric cap on the non-crystalline metallic silicide film. The at least one gate stack is formed on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting. It is respectfully submitted that the Chen reference, in the first embodiment disclosed therein, fails to describe, either expressly or inherently, at least one gate stack comprising, in part, a dielectric cap on a crystalline metallic silicide film. Further, a gate stack formed on a silicon substrate having a dielectric layer thereover, the dielectric layer being substantially devoid of pitting, is not disclosed, either expressly or inherently, in the second embodiment of the Chen reference. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched prior to implanting the metal silicide

layer and transforming it back to the amorphous state. As such, it is respectfully submitted that the Chen reference fails to anticipate amended independent claim 29.

Independent claim 31, as amended herein, recites a semiconductor device comprising at least one gate stack structure on a dielectric layer, over a silicon substrate, wherein the dielectric layer is substantially devoid of pitting, the at least one gate stack structure comprising a metallic silicide film and a dielectric cap on the metallic silicide film. The Chen reference, in the first embodiment disclosed therein, fails to describe, either expressly or inherently, at least one gate stack comprising a dielectric cap on a metallic silicide film as recited in amended independent claim 31. Further, the Chen reference, in the second embodiment described therein, fails to disclose, either expressly or inherently, a gate stack structure on a dielectric layer wherein the dielectric layer is substantially devoid of pitting. Rather, the dielectric layer of the structure of the second embodiment includes pitting as the gate electrode structure is etched prior to implanting the metal silicide layer and transforming it back to the amorphous state. Accordingly, it is respectfully submitted that the Chen reference fails to anticipate amended independent claim 31.

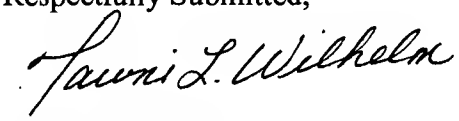
In light of the above, it is respectfully submitted that the Chen reference fails to disclose, either expressly or inherently, each and every element of amended independent claims 23, 24, 25, 26, 29 and 31. As such, these claims are not anticipated by the Chen reference and withdrawal of the 35 U.S.C. §102(e) rejection thereof is respectfully requested. Each of these claims is believed to be in condition for allowance and such favorable action is respectfully requested.

Claims 27 and 28 each depend from claim 26, claim 30 depends from claim 29 and claims 32 and 33 each depend from claim 31. Accordingly, each of these claims is believed to be in condition for allowance for at least the above-cited reasons. As such, withdrawal of the 35 U.S.C. § 102(e) rejection of these claims is respectfully requested.

CONCLUSION

Claims 23 through 33 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,



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TLW/ah
Enclosure: Version of Claims with Markings to Show Changes Made
Petition for One-Month Extension of Time
Check No. 18651 in the amount of $110.00.

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VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

23. (Thrice Amended) An operable gate stack on a silicon substrate having a dielectric layer thereover, said dielectric layer being substantially devoid of pitting, said operable gate stack including a non-crystalline metallic silicide film and a dielectric cap on said non-crystalline metallic silicide film.

24. (Four Times Amended) An operable gate stack on a silicon substrate having a dielectric layer thereover, said dielectric layer being substantially devoid of pitting, said operable gate stack including an amorphous metallic silicide film, wherein said amorphous metallic silicide film is substantially devoid of silicon clusters, and a dielectric cap on said amorphous metallic silicide film.

25. (Five Times Amended) An operable gate stack on a silicon substrate having a dielectric layer thereover, said dielectric layer being substantially devoid of pitting, said operable gate stack comprising:
a polysilicon layer disposed over said dielectric layer;
a non-crystalline metallic silicide film disposed over said polysilicon layer; and
a dielectric cap on said non-crystalline metallic silicide film.

26. (Four Times Amended) A gate stack structure comprising an operable gate stack on a dielectric layer, over a silicon substrate, wherein said dielectric layer is substantially devoid of pitting, said operable gate stack comprising a metallic silicide film and a dielectric cap on said metallic silicide film.

27. (Four Times Amended) The gate stack structure of claim 26, wherein said ~~operable gate stack includes~~metallic silicide film comprises a non-crystalline metallic silicide film.

28. (Thrice Amended) The gate stack structure of claim 26, wherein said ~~operable gate stack includes~~metallic silicide film comprises an amorphous metallic silicide film substantially devoid of silicon clusters.

29. (Amended) A semiconductor device, comprising at least one gate stack ~~having~~ formed on a silicon substrate having a dielectric layer thereover, said dielectric layer being substantially devoid of pitting, said at least one gate stack comprising a non-crystalline metallic silicide film and a dielectric cap on said non-crystalline metallic silicide film.

30. (Amended) The semiconductor device of claim 29, wherein said at least one gate stack further comprises~~:~~

~~a silicon substrate having a dielectric layer thereover;~~

a polysilicon layer disposed over said dielectric layer~~;~~,

~~a~~said non-crystalline metallic silicide film being disposed over said polysilicon layer~~; and a dielectric cap on said non-crystalline metallic silicide film~~.

31. (Amended) A semiconductor device, comprising at least one gate stack structure on a dielectric layer, over a silicon substrate, wherein said dielectric layer is substantially devoid of pitting, said at least one gate stack structure comprising a metallic silicide film and a dielectric cap on said metallic silicide film.

32. (Amended) The semiconductor device of claim 31, wherein said ~~at least one gate stack structure includes~~metallic silicide film comprises a non-crystalline metallic silicide film.

33. (Amended) The semiconductor device of claim 31, wherein said ~~at least one gate stack structure includes~~metallic silicide film comprises an amorphous metallic silicide film substantially devoid of silicon clusters.